Chapter 4
Designing with LVDS

4.1 Introduction

LVDS has low-swing, differential, ~3.5 mA current-mode outputs that can help reduce noise/EMI significantly, but these outputs switch (rise and fall) in less than a nanosecond, which means that almost every interconnect will act as a transmission line. Therefore, knowledge of ultra-high-speed board design and differential signal theory is required. Designing high-speed differential boards is not difficult or expensive. So familiarize yourself with the techniques outlined in Chapter 3 before you begin your design.

4.1.1 High-speed layout

See Chapter 3.

4.1.2 Unused pins

LVDS inputs - Leave unused LVDS receiver inputs open (floating) for LVDS receivers unless directed differently by the specific component's datasheet. Their internal failsafe feature will provide sufficient biasing to put the outputs in a known state. These unused receiver inputs should not be connected to noise sources such as cables or long PCB traces - float them near the pin. LVDS receivers are high-speed, high-gain devices, and only a small amount of noise, if picked up differentially will cause the receiver to respond. This causes false transitions on the output and increases power consumption.

LVDS and TTL outputs - Leave all unused LVDS and TTL outputs open (floating) to conserve power. Do not tie them to ground.

TTL inputs - Tie unused TTL transmitter/driver inputs and control/enable signals to power or ground or in certain cases they may be left open if the datasheet supports this condition. Some devices provide internal pull down (or up) devices to bias the pins. Again, consult the datasheet for information regarding the device's features. This type of information is typically included in the pin description table.

4.1.3 Probing LVDS transmission lines

Always use a high impedance (>100 k Ω), low capacitance (<0.5 pF) probe/scope with a wide bandwidth (>1 GHz). Improper probing will give deceiving results. LVDS is not intended to be loaded with a 50 Ω load to ground. This will distort the differential signal and offset voltages of the driver.

Differential probes are recommended over two standard scope probes due to match and balance concerns. Probe/scope combinations should have enough bandwidth to properly monitor the signal. Tektronix and Agilent (HP) both make probes that are well suited for measuring LVDS signals. (See Chapter 7)

4.1.4 Loading LVDS I/O – preserving balance

Avoid placing any devices which heavily load the low, ~3.5 mA LVDS output drive. If additional ESD protection devices are desired, use components, which do not add a significant load to the LVDS output. Some of the connectors with integrated polymer ESD protection are a good option.

Try not to disturb the differential balance. Treat both members of a pair equally.

4.2 Results of good vs. bad design practices

4.2.1 Impedance mismatches

It is very common for designers to automatically use off-the-shelf cables and connectors and 50Ω autorouting when making new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low-swing, current-mode outputs designed to reduce noise. However, the transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable are not meant for high-speed signals (especially differential signals) and do not always have controlled impedance.

Figure 4.1 shows a time-domain reflectometer (TDR) impedance trace of such a system. As one can plainly see, impedances are neither matched nor controlled. This example is not the worst case – it is a typical example reflecting common TTL design practices. The reflections caused by impedance mismatching will generate a lot of noise and EMI.

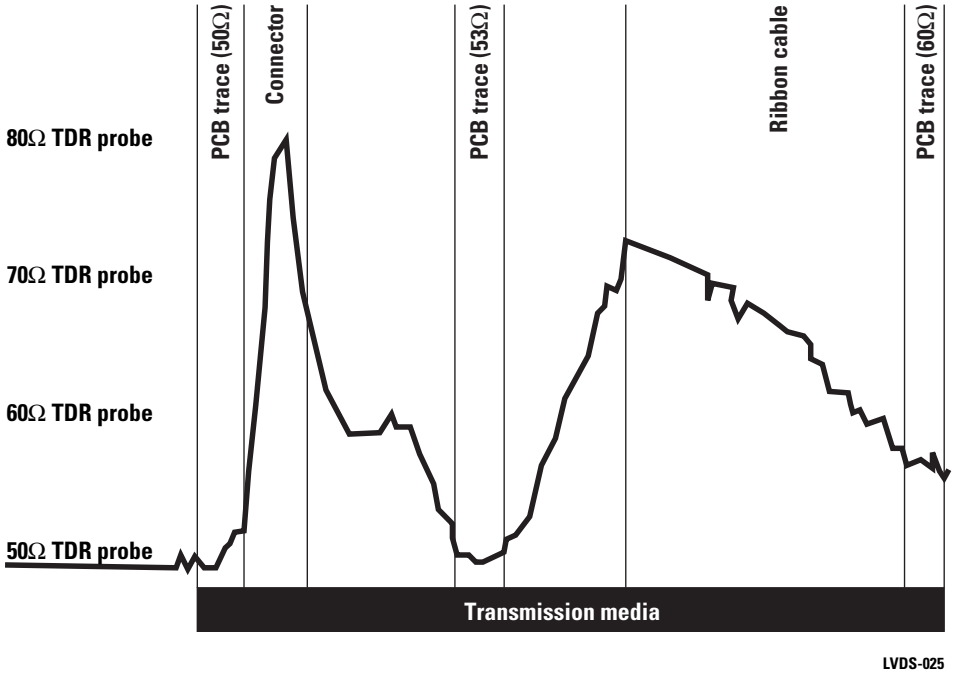

Figure 4.1. TDR plot of transmission media with mismatched impedance

Figure 4.2 is a trace of an improved design that follows most of the high-speed differential design practices discussed in Chapter 3. The TDR differential impedance plot is much flatter and noise is dramatically reduced.

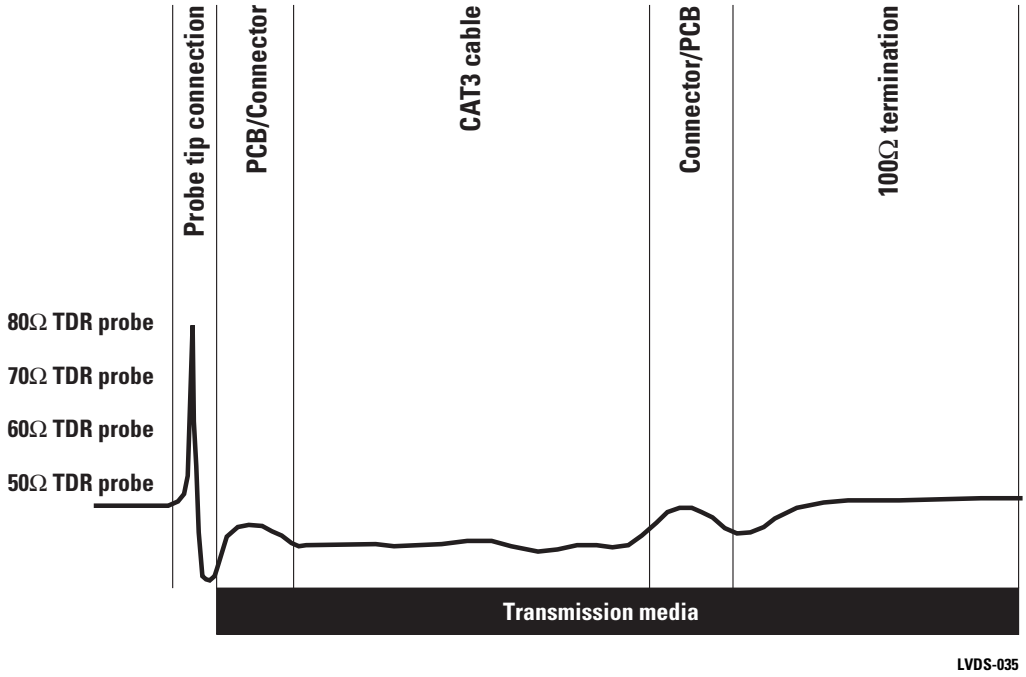

Figure 4.2. Minimize impedance variations for best performance

4.2.2 Crosstalk between TTL and LVDS signals

Figure 4.3 and 4.4 show the effects of TTL coupling onto LVDS lines. Figure 4.3 shows the LVDS waveforms before coupling. The second shows the effects of a 25 MHz, 0V to 3V TTL signal upon the LVDS signals running adjacent for 4 in. The result is an LVDS waveform modulated by the TTL signal. Note that the LVDS pair is not affected exactly equally – the signal which runs closest to the TTL trace is affected more than the other. The receiver will not reject this difference as common-mode noise. While it will not falsely trigger the receiver, it does degrade the signal quality of the LVDS signal and reduce noise margin. The common-mode noise will be rejected by the receiver, but can radiate as EMI.

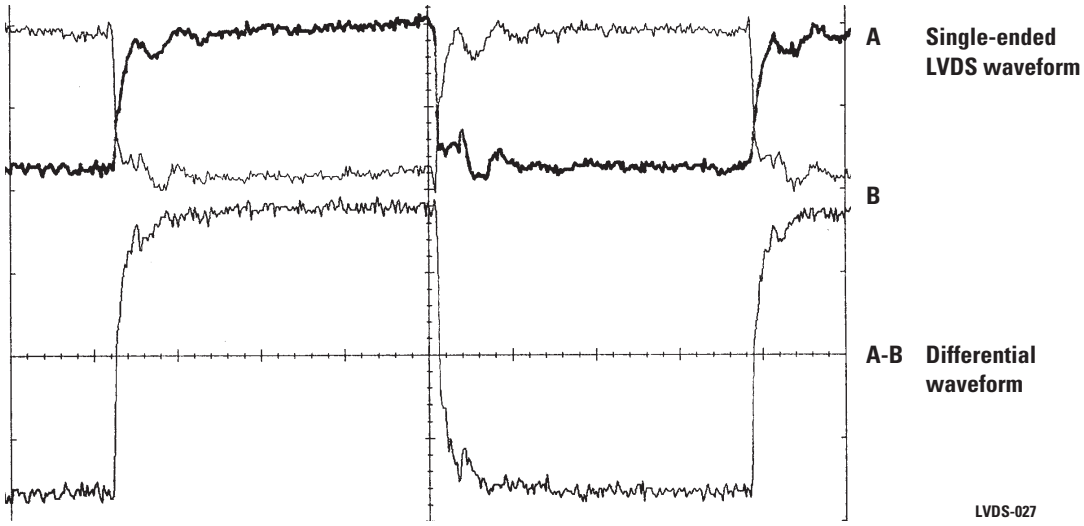

Figure 4.3. LVDS signals before crosstalk

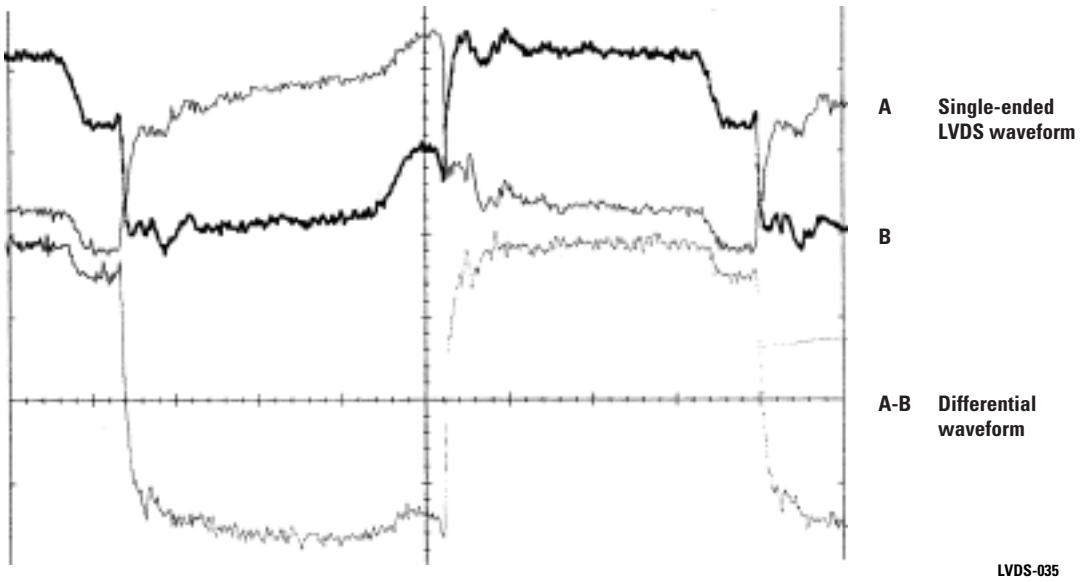

Figure 4.4. LVDS signals affected by TTL crosstalk

4.2.3 Interfacing LVDS backplane drivers with FPGAs

There is a simple but common mistake that many designers make when interfacing their LVDS ICs with their FPGAs (or ASICs). They overdrive the single-ended signal from the FPGA into the LVTTL I/O of the LVDS transmitter.

Many FPGAs are capable of driving signals over short backplanes. For that purpose, the output driver can be set to drive large amplitude signals, perhaps even with pre-emphasis. When that large signal is sent over only 3 to 6 in. of FR4 to the input stage of an LVDS buffer, it will cause problems.

The designer should avoid saturating the inputs of backplane drivers by lowering the signal amplitudes from the FPGA.

4.3 Lowering Electromagnetic Interference (EMI)

4.3.1 LVDS and lower EMI

High-speed data transmission usually means fast edge rates and high EMI. LVDS, however, has many positive attributes that help lower EMI:

1. The low output voltage swing (~350 mV)
2. Relatively slow slew rates, $\frac{\Delta V}{\Delta t} \sim \frac{0.350V}{0.350\,ns} = 1\text{V / ns}$
3. Differential (odd mode operation) so magnetic fields tend to cancel
4. “Soft” output corner transitions
5. Minimum ICC spikes due to low current-mode operation and internal circuit design

To realize these advantages, however, designers must take care to ensure the close proximity of the pair conductors and to avoid creating impedance imbalances within a pair. The following sections describe these EMI-friendly design practices.

4.4 Common-mode noise rejection

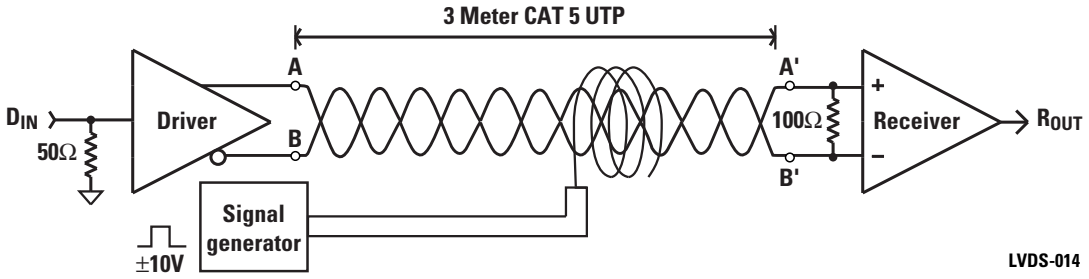

Figure 4.5. Common-mode noise rejection test setup

Test setup:

- Driver: DS90C031 (one channel)
- Receiver: DS90C032 (one channel)
- V_{CC} = 5V
- T_A = 25°C

This test demonstrates the common-mode noise rejection ability of National's LVDS receivers. Some have expressed concern over the noise immunity of LVDS because of its low voltage swing (±350 mV swing with <±100 mV thresholds). Provided that the differential signals run close together through controlled impedance media, most of the noise on LVDS lines will be common-mode. In other words, EMI, crosstalk, and power/ground shifts will appear equally on each pair and this common-mode noise will be rejected by the receiver. The plots below show common-mode noise rejection with V_{CM} noise up to –0.5V to +3.25V peak-to-peak.

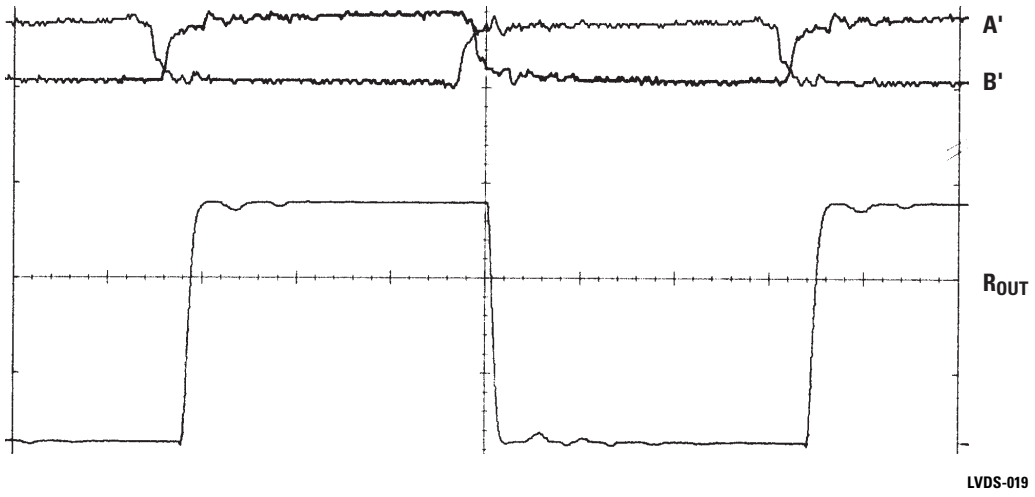

Figure 4.6. Reference waveform showing LVDS signal and receiver output

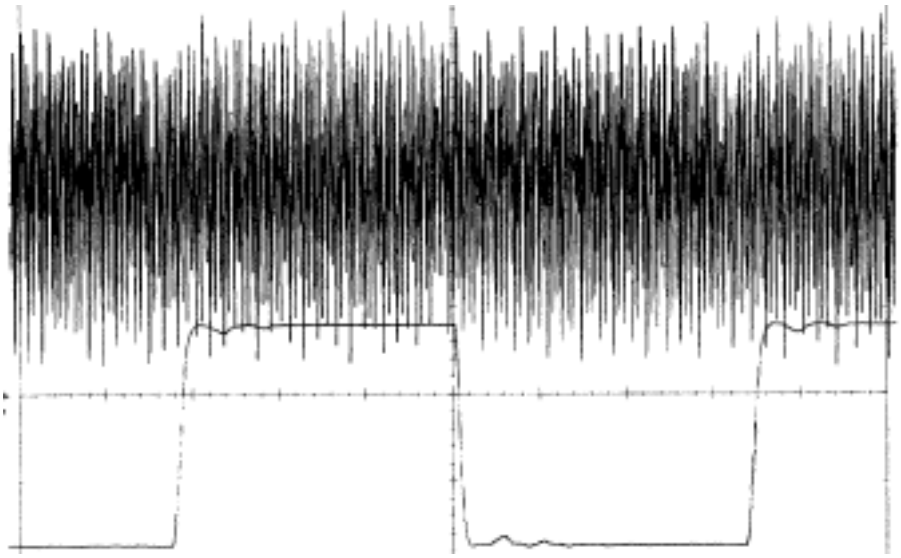

Figure 4.7. Coupled common-mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output

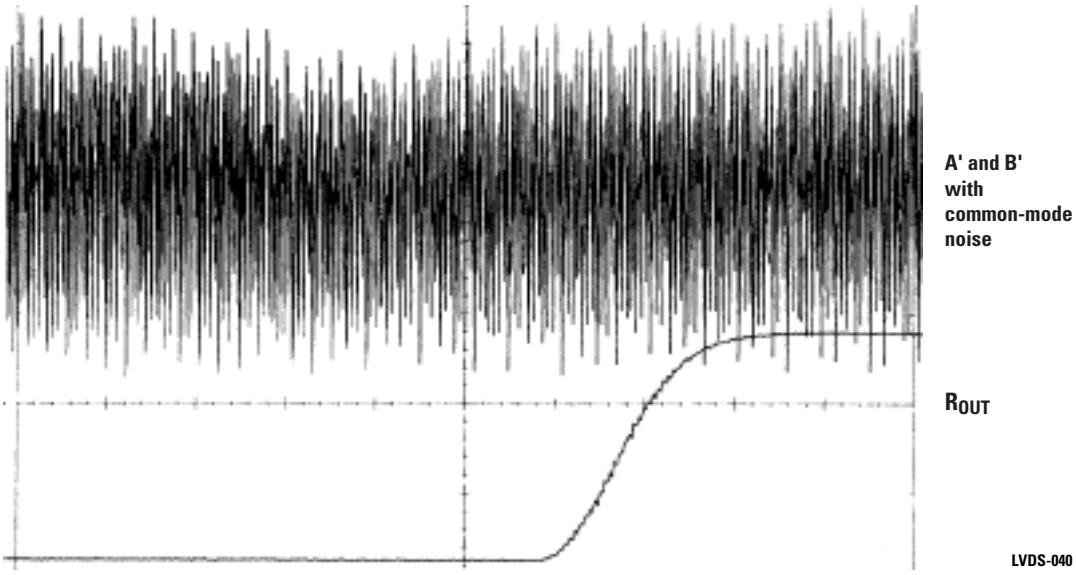

Figure 4.8. Expanded view of coupled common-mode noise waveform and clean receiver output

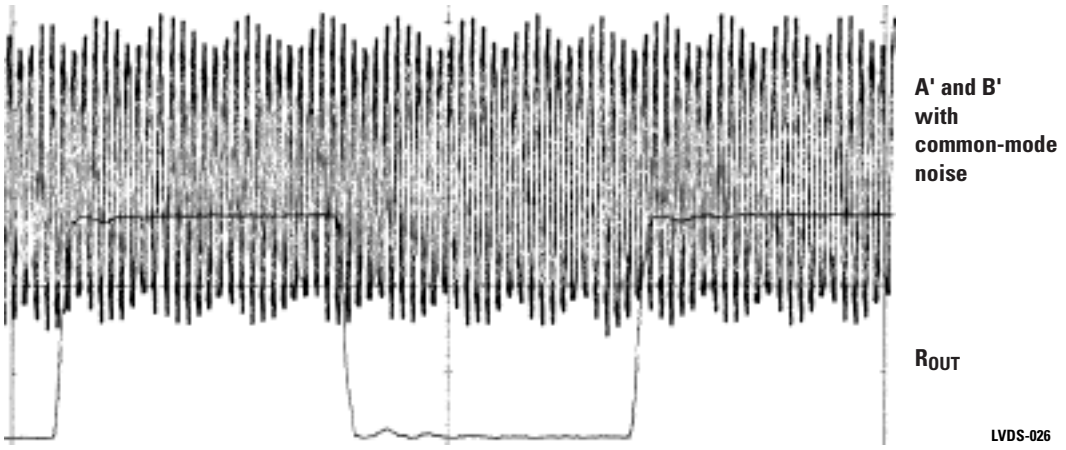

Figure 4.9. Clean receiver output despite –0.5V to +3.25V peak-to-peak common-mode noise

4.5 LVDS configurations

Unlike many other technologies such as ECL and CML which are more limited in configurations, LVDS has many possible configurations.

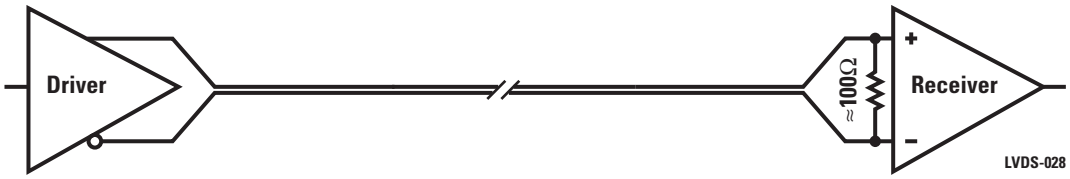

Figure 4.10. Point-to-point configuration

LVDS drivers and receivers are typically used in a point-to-point arrangement (Figure 4.10), but other topologies are possible. The point-to-point configuration does provide the best signal path and should be used for very high-speed interconnect links. Point-to-point links are commonly used in conjunction with crosspoint switches.

The configuration shown in Figure 4.11 allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin) if using standard LVDS drivers. A better solution would be to employ Bus LVDS drivers, which are designed for double termination loads. The simplest configuration for bi-directional communication is to implement a LVDS or Bus LVDS transceiver. They provide levels compatible with LVDS and do not trade off noise margin. Common-mode range for LVDS and Bus LVDS is ±1V (typical), so cable lengths tend to be in the tens of meters.

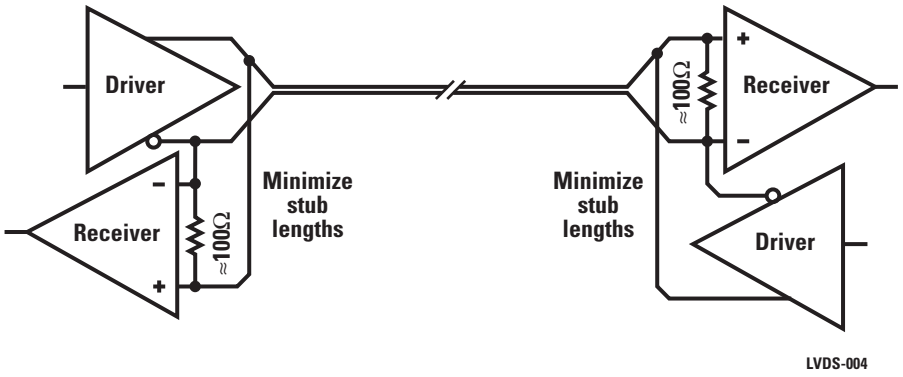

Figure 4.11. Bi-directional half-duplex configuration

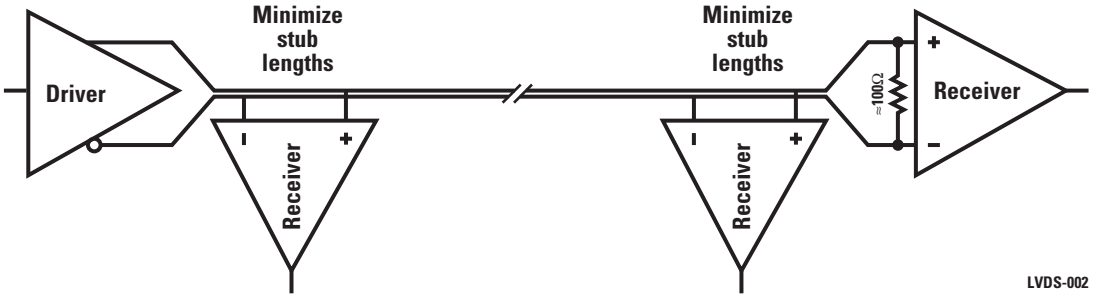

Figure 4.12. Multidrop configuration

LVDS receivers have high impedance inputs, so a multidrop configuration can also be used. A multidrop configuration will be most effective when transmission distance is short and stub lengths are less than ~15 mm (as short as possible). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down. This application is good when the same set of data needs to be distributed to multiple locations.

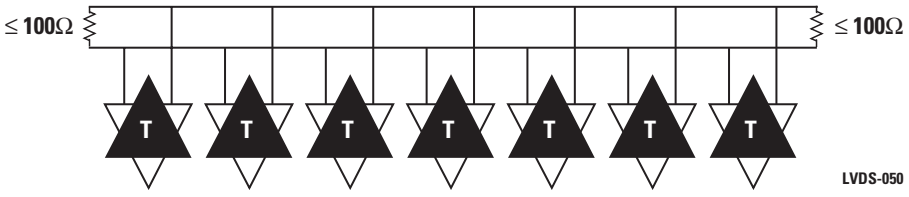

Figure 4.13. Multipoint configuration

A multipoint bus supports multiple drivers, but only one is allowed to be active at any given time.

With Bus LVDS devices, double terminated busses can be used without trading off signal swing and noise-margin. Termination should be located at both ends of the bus. Failsafe biasing should be considered if a known state on the bus is required when all drivers are in TRI-STATE®. When a designer is working with the multidrop bus, he should keep stubs off the mainline as short as possible, and he should pay special attention to device edge-rate specifications. Faster edge-rates will increase transmission line effects caused by long stubs.

4.6 Failsafe biasing of LVDS

4.6.1 Most applications

Most LVDS receivers have internal failsafe circuitry that forces the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, and terminated receiver inputs. Always consult the component's datasheet to determine which type of failsafe protection is supported. Here is a summary of LVDS failsafe conditions:

Open input pins - Unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal failsafe bias resistors will pull the "+" input high, and the "–" input low, thus guaranteeing a high, stable output state. This minimizes power dissipation and switching noise.

Terminated input pins - If the cable is removed and the inputs to the receiver have a termination resistor across them, then the output will be stable (HIGH). Noise picked up at the input, if differential in nature, can cause the device to respond. If this is the case see Section 4.6.2.

Terminated input pins - Noisy Environments - See Section 4.6.2 if failsafe must be guaranteed in noisy environments when the cable is disconnected from the driver's end or if the driver is in TRI-STATE.

Shorted inputs - The receiver output will remain in a high state when the inputs are shorted. This is considered a fault condition protection only. It is not specified across the input voltage range of the receiver.

With some devices, such as National's Bus LVDS family of devices, outputs may also be in other states, such as TRI-STATE, when used in the configurations stated above. Please consult the specific device's datasheet for details.

4.6.2 Boosting failsafe in noisy environments

The internal failsafe circuitry is designed to source/sink a very small amount of current, providing failsafe protection for floating receiver inputs, shorted receiver inputs and terminated receiver inputs as described above and in the component's datasheet.

It is not designed to provide failsafe in noisy environments when the cable is disconnected from the driver or receiver's end or if the driver is in TRI-STATE. When this happens, the cable can become a floating antenna, which can pick up noise. If the cable picks up more differential noise than the internal failsafe circuitry can overcome, the receiver may switch or oscillate. If this condition occurs in your application, it is recommended that you choose a balanced and/or shielded cable, which will reduce the amount of differential noise on the cable.

In addition, you may wish to add external failsafe resistors to create a larger noise margin. However, adding more failsafe current will tend to unbalance the symmetrical LVDS output drive (loop) current and degrade signal quality somewhat. Therefore, a compromise should be the ultimate goal.

4.6.3 Choosing external failsafe resistors

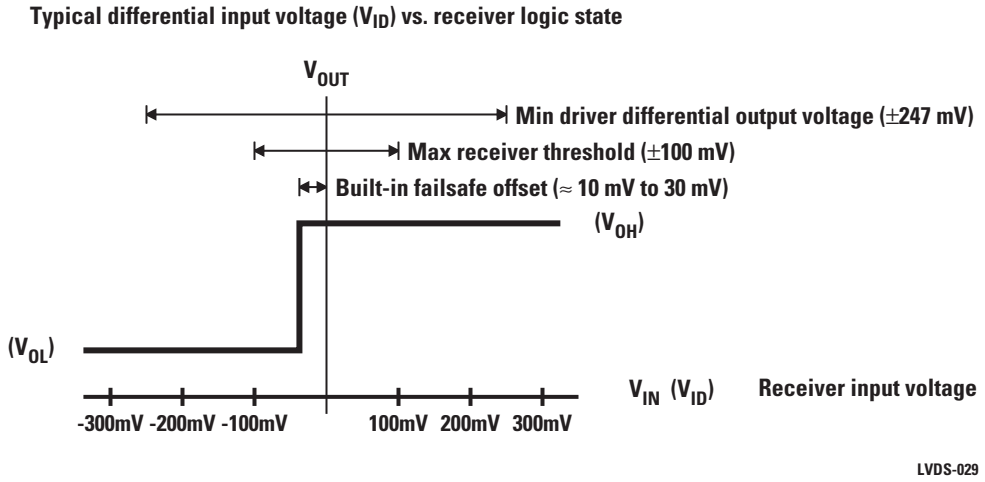

Figure 4.14. External failsafe can be added, but must be small enough not to significantly affect driver current

Figure 4.14 shows that National's present LVDS devices typically have an internal failsafe voltage of about -10 mV to 30 mV. If the driver in your application will not always actively drive the receiver and the cable is expected to pick up more than 10 mV of differential noise, you may need to add additional failsafe resistors.

The resistors are chosen by first measuring/predicting the amount of differential-mode noise you will need to overcome. V_{FSB} is the offset voltage generated across the termination resistor (typically 100Ω). Note that you do not need to provide a bias (V_{FSB}) that is greater than the receiver threshold (100 mV). Typically +15 mV or +20 mV is sufficient. You only need enough to overcome the differential noise, since the internal failsafe circuitry will always guarantee a positive offset. In fact, making V_{FSB} too large will contend with the driver output causing the driven signal to become imbalanced and reduce signal quality.

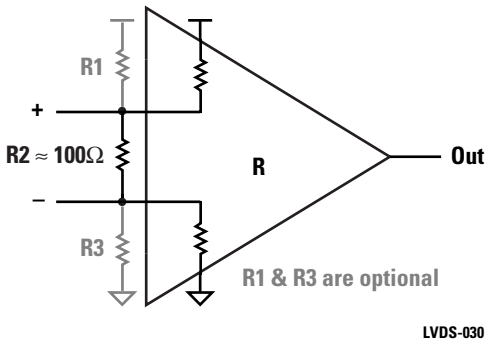

Figure 4.15. Simplified internal failsafe circuitry and optional external "helper" failsafe resistors

For best results, follow these procedures when choosing external failsafe resistors:

1. First ask the question "Do I need external failsafe?" If your LVDS driver is always active, you will not need external failsafe. If the cable is never disconnected from the driver end while the system is active and/or your cable will not pick up much differential-mode noise, you may not need to boost failsafe. If you have a noisy backplane application where the driver does not always drive the receiver, or if the driver card can be unplugged, then you may need additional failsafe biasing.

2. Measure/predict the amount of differential-mode noise at the receiver end of the cable in worst-case conditions. If you measure a great deal of noise, use a balanced cable such as twisted pair cabling. UTP cables tends to mostly pick up common-mode noise and not differential-mode noise. Do not use simple ribbon cables that can pick up differential-mode noise due to fixed positions of the conductors.

   Use a shielded cable whenever possible. Using a balanced and/or shielded cable is the best way to prevent noise problems in noisy environments.

3. Once you have chosen the appropriate cable, measure the amount of differential voltage at the receiver under worst-case conditions. Set this equal to V_{FSB} in the equation below and solve for the external failsafe resistors R1 and R3.

4. You now have an equation relating R1 to R3. Choose R1 and R3 so that: (1) they approximately satisfy the third equation for V_{CM} = 1.2V, and (2) they are large enough that they do not create a bias which will contend with the driver current (I_{BIAS} << I_{LOOP}, equation two). In general, R1 and R3 should be greater than 20 kΩ for V_{CC} = 5V and greater than 12 kΩ for V_{CC} = 3.3V. Remember that you want just enough I_{BIAS} to overcome the differential noise, but not enough to significantly affect signal quality.

5. The external failsafe resistors may change your equivalent termination resistance, R_{TEQ}. Fine-tune the value of R2 to match R_{TEQ} to within about 10% of your differential transmission line impedance.

See AN-1194 - Failsafe Biasing of LVDS Interfaces

4.7 Power-off high-impedance bus pins

Power-off high-impedance is a useful feature; most second and third generation LVDS receivers provide this feature. This is typically listed as a feature and also as a condition of the I_{IN} parameter. This feature is useful in applications that employ more than one receiver and they are powered from local power supplies. If the power is turned off to one node, it should not load down the line and prevent communication between other powered-up nodes.