

## STRUCTURE TYPE

Silicon Monolithic Integrated Circuit  
Flexible Step-Down Switching Regulator

## PRODUCT SERIES

**BD9778HFP**

## FEATURES

- Wide input Range:7~35V
- High Precision(Reference Voltage) :  $\pm 2\%$
- Integrated 2A P-ch Power MOS FET
- Adjustable Frequency:50~500KH z

### ○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	$V_{IN}$	36	V
SW Pin Voltage	$V_{SW}$	$V_{IN}$	V
Output SW Current	$I_{SW}$	2 <sup>(1)</sup>	A
EN Pin Voltage	$V_{EN}$	$V_{IN}$	V
RT, FB, INV Pin Voltage	$V_{RT}, V_{FB}, V_{INV}$	7	V
Power Dissipation	$P_d$	5.5 <sup>(2)</sup>	W
Operating Temperature Range	$T_{opr}$	-40 ~ +125	°C
Storage Temperature Range	$T_{stg}$	-55 ~ +150	°C
Maximum Junction Temperature	$T_{jmax}$	150	°C

(1) Do not however exceed  $P_d$ .

(2)  $P_d$  derated at 44mW/°C for temperature above Ta=25°C, Mounted on a double layer PCB 70mm×70mm×1.6mm.  
(with Thermal vias / Copper area : 70mm×70mm)

### ○ OPERATING CONDITIONS(Ta=25°C)

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	$V_{IN}$	5	35	V
Recommend Supply Voltage	$V_{IN}$	7	35	V
Output Switch Current	$I_{SW}$	-	2	A
Oscillator Frequency	$F_{OSC}$	50	500	kHz
Oscillator Timing Resistance	RT	40	800	kΩ
Output Voltage *1	$V_o$	1 or $V_{IN} \times 6\%$	$V_{IN}$	V

※Electrical characteristics are not guaranteed (especially when operating on reduce voltage)

\*1 This Output Voltage is applied to Recommend Supply Voltage (7~35V)

\* The product described in this specification is a strategic product (and/or Service) subject to COCOM regulations. It should not be exported without Authorization from the appropriate government.

\* The product is not designed for protection against radioactive rays.

\* Status of this document

The Japanese version of this document is the formal specification.

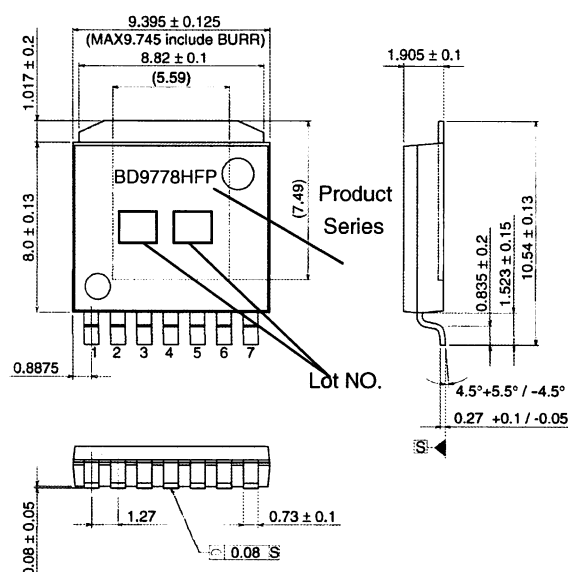
A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

○ ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=-40~125℃, V<sub>IN</sub>=13.2V, V<sub>EN</sub>=5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
[Entire Device]						
Stand-by Current	I <sub>STB</sub>	-	0	10	μA	V <sub>EN</sub> =0V, Ta=25℃
Quiescent Current	I <sub>Q</sub>	-	3	4.2	mA	I <sub>O</sub> =0A
[Switch]						
Switch On Resistance	R <sub>ON</sub>	-	0.53	0.9	Ω	I <sub>SW</sub> =50mA
Output Current Limit	I <sub>OLIMIT</sub>	2	4	-	A	Design Guarantee
Leakage Current	I <sub>OLEAK</sub>	-	0	30	μA	V <sub>IN</sub> =35V, V <sub>EN</sub> =0V
[Error Amplifier]						
Reference Voltage1	V <sub>REF1</sub>	0.98	1.00	1.02	V	V <sub>FB</sub> =V <sub>INV</sub> , Ta=25℃, S:ON,
Reference Voltage2	V <sub>REF2</sub>	0.96	1.00	1.04	V	V <sub>FB</sub> =V <sub>INV</sub> , S:ON
Line Regulations	ΔV <sub>REF</sub>	-	0.5	-	%	V <sub>IN</sub> =5 ~35V, S:ON
Input Bias Current	I <sub>B</sub>	-1	-	-	μA	V <sub>INV</sub> =1.1V
Maximum FB Voltage	V <sub>FBH</sub>	2.4	2.5	-	V	V <sub>INV</sub> =0.5V
Minimum FB Voltage	V <sub>FBL</sub>	-	0.05	0.10	V	V <sub>INV</sub> =1.5V
FB sink current	I <sub>FBSINK</sub>	-5.0	-3.0	-0.5	mA	V <sub>FB</sub> =1.5V, V <sub>INV</sub> =1.5V
FB source current	I <sub>FBSOURCE</sub>	70	120	170	μA	V <sub>FB</sub> =1.5V, V <sub>INV</sub> =0.5V
Soft Start Period	T <sub>SS</sub>	-	5	-	mS	Design Guarantee
[Oscillator Section]						
Switching Frequency	F <sub>OSC</sub>	82	102	122	kHz	RT=390kΩ
Frequency Line Regulation	ΔF <sub>OSC</sub>	-	2	-	%	V <sub>IN</sub> =5~35V
[Enable]						
Enable Threshold Voltage	V <sub>EN</sub>	0.8	1.7	2.6	V	
Sense Current	I <sub>EN</sub>	-	13	50	μA	V <sub>EN</sub> =5V

○ PHYSICAL DIMENTIONS • MARKING



HRP7 (UNIT:mm)

The diagram illustrates the internal control logic of a switching regulator. It features several key components and their interconnections:

- Inputs:**  $V_{IN}$  (pin 1),  $INV$  (pin 5),  $FB$  (pin 3), and  $GND$  (pin 4).
- Outputs:**  $EN$  (pin 7) and  $SW$  (pin 2).
- Control Logic:**
  - ON/OFF:** A block that controls the  $EN$  pin. It has two states:  $L:OFF$  and  $H:ON$ .
  - SOFT START:** A block that provides a ramp to the  $ERROR\ AMP$ .
  - ERROR AMP:** An operational amplifier that compares the  $FB$  signal with a reference voltage ( $V_{ref}$ ) and provides a signal to the **PWM COMPARATOR**.
  - PWM COMPARATOR:** A comparator that generates a **PWM** signal based on the  $ERROR\ AMP$  output and a sawtooth wave from the **OSC** block.
  - LATCH:** A block that latches the **PWM** signal and provides a **RESET** signal to the **OSC** block.
  - DRIVER:** A block that drives the **SW** pin based on the **PWM** signal and a **TSD** (thermal shutdown) signal.
  - TSD:** A thermal shutdown block that resets the **LATCH** if the device overheats.
  - CURRENT LIMIT:** A block that monitors the  $V_{IN}$  and provides a **RESET** signal to the **LATCH** if the current limit is reached.
- Other Components:** **OSC** (oscillator) and **Vref** (reference voltage) are also shown.

※Refer to the Technical Note about the details of the application.

Pin No.	Pin Name
1	VIN
2	SW
3	FB
4	GND
5	INV
6	RT
7	EN
FIN	FIN

## NOTES FOR USE

### 1. Absolute maximum range

Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed we cannot be defined the failure mode, such as short mode or open mode.

Therefore physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

### 2. Operation supply voltage range

The circuit functionality is guaranteed within operation of ambient temperature range, as long as it is within operation supply voltage range. The standard electrical characteristic values are guaranteed at the test circuit voltage of  $V_{IN}=13.2V$ . They cannot be guaranteed at other voltages in the operating range of 5V-35V. However, the variation will be small.

### 3. Grounding

It is recommended that every capacitor (bypass and another capacitors) is grounded to PIN7 using single-point connections.

### 4. Input supply voltage

Input supply pattern layout should be as short as possible.

### 5. VIN Terminal

For reduce the influence of switching noise, bypass capacitor is connected between VIN and GND.

### 6. FB Terminal

The FB terminal is for phase margin of the DC/DC system. A capacitor and a resistor or an only capacitor placed between the FB terminal and the INV terminal. The values of the capacitor and the resistor shall be adjusted according to the output current and the output capacitor value. The output may be oscillating if the value of capacitor is not sufficient, also the transient response may become insufficient if the value is too large. Therefore, the value of the capacitor and the resistor shall be adequately set up based on the condition of the temperature, and so on. Since the FB terminal also detects output short condition compulsorily applying an external voltage onto the FB terminal must not be performed because it may activate the timer latch protection circuit.

### 7. Electromagnetic Fields

The IC is susceptible to strong electromagnetic fields and may cause malfunction. Therefore, caution should be used when placing it on the PCB.

### 8. Application Design

When designing the external circuit, included adequate margins, including not only steady state but also transient characteristics.

### 9. Over Output Current Protection

SW Output terminal has over current protection circuit of 4A, with prevents IC from being damage by short circuit at over current.

### 10. Thermal Shut Down Circuit

A temperature control is built in the IC to prevent the damage due to overheat. Therefore, the output is turned off when the thermal circuit works and are turned on when the temperature goes down to the specified level.

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